WHAT IS CLAIMED IS:

1. A circuit for producing a time-delayed transmitted reference spread spectrum signal comprising:

first and second shift registers having primitive polynomial feedback circuits;

a delay module connected to the output of the first shift register;

a modulator connected to an output of said delay module;

a narrowband message signal connected to said modulator;

a summer connected to an output of the second shift register; and

wherein an output of said modulator connected to said summer, and wherein the summer produces the time-delayed transmitted reference spread spectrum signal as an output.

2. The circuit of Claim 1 wherein the first and second shift registers each have the same bit size capacity.

3. The circuit of Claim 1 wherein the first and second shift registers each comprise a bit size capacity of at least four bits.

4. The circuit of Claim 1 wherein the first and second shift registers are preset wherein each have a first predetermined setting and wherein the first and second shift registers are each run at a predetermined clock rate.

5. The circuit of Claim 4 wherein the delay module comprises a delta (δ) stage shifter register.

6. The circuit of Claims 5 wherein the delta (δ) stage shift register is clocked at the predetermined clock rate.

7. The circuit of Claim 1 wherein the polynomial feedback circuits comprise a first exclusive-or logic gate connected to the first shift register and a second exclusive-or logic gate connected to the second shift register.

8. A circuit for producing a time-delayed transmitted reference spread spectrum signal comprising:

a shift register having a primitive polynomial feedback circuit;

a modulo-two adder connected to predetermined bits of said shift register;

a modulator connected to an output of said modulo-two adder;

a narrowband message signal connected to said modulator; and

a summer connected to an output of said modulator and a sequence generated by said shift register wherein an output of the summer produces the time-delayed transmitted reference spread spectrum signal.

9. The circuit of Claim 8 wherein the shift register comprises a bit size capacity of at least four bits.

10. The circuit of Claim 8 wherein the primitive polynomial feed back circuit comprises an exclusive-or gate.

11. The circuit of Claim 8 wherein the shift register comprises a bit size of four bits.

12. The circuit of Claim 11 wherein the modulo-two adder is connected a first, second and third bit of the shift register.

13. The circuit of Claim 11 wherein the polynomial feedback circuit is connected to the first and second bits of the shift register.

14. The circuit of Claim 11 wherein an output of the polynomial feedback circuit is connected to an output of the shift register.

15. A circuit for producing a time-delayed transmitted reference spread spectrum signal comprising:

a plurality of end-around circulating shift registers;

a control circuit connected to the plurality of end-around circulating shift registers for controlling a circulation of bits in said end-around circulating shift registers; and

a sampling circuit connected predetermined ones of the plurality of the end-around circulating shift registers for sampling the predetermined end-around circulating shift registers, said sampling being chosen to provide a noise-like digital sequence and its delayed replica for producing the time-delayed transmitted reference spread spectrum signal.

16. The circuit of Claim 15 wherein the sampling circuit twice samples the end-around circulating shift registers.

17. The circuit of Claim 15 wherein the control circuit comprises a plurality of component register clocks wherein each of the plurality of component register clocks are individually connected to unique ones of the plurality of end-around shift registers.

18. The circuit of Claim 15 wherein the sampling circuit comprises a first and second rotating selector.

19. The circuit of Claim 18 wherein said first rotating selector is delayed a predetermined time from said second rotating selector.

20. The circuit of Claim 18 wherein an output of the first rotating selector is connected to a modulator, said modulator being connected to a narrow band

message signal wherein an output of said modulator and an output of said second rotating selector are connected to a combiner.